is generated so as to deteriorate the yield, which is problematic.

Page 2, replace the paragraph, beginning on line 22, as follows:

Accordingly, an object of the present invention is to provide a novel semiconductor device with an improved yield by solving the problems in the above-mentioned conventional technology, in particular, by shortening the wire length per one loop so as to eliminate the problems of wire sagging by its own weight, tilting of the wire at the time of sealing, or the like.

Page 6, replace the paragraph, beginning on line 18, as follows:

The second embodiment comprises the semiconductor device shown in FIG. 2, wherein relaying pads 71a, 71b are connected electrically by a wiring 72 in the inner layer of a polyimide tape 7.

IN THE CLAIMS:

Cancel claims 1-6.

Add the following new claims:

7. (new) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second

semiconductor chips, said wiring layer including a polyimide tape having a copper foil layer therein;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other.

--8. (new) The semiconductor device according to claim 7, wherein,

a first bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said first semiconductor chip;

a second bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said wiring layer; and

a third bonding wire connects said one of said plural bonding pads on said wiring layer to one of said plural bonding pads on said second semiconductor substrate.

--9. (new) The semiconductor device according to claim 7, further comprising a connection wire for connecting said one of said plural bonding pads on the wiring layer to another one of said plural bonding pads on said wiring layer.

--10. (new) The semiconductor device according to claim 7, further comprising a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding

pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

--11. (new) The semiconductor device according to claim 9, further comprising a via hole in said wiring layer, said via hole having a contact for connecting yet another one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

--12. (new) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a conductor within said wiring layer;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other.

--13. (new) The semiconductor device according to claim 12, wherein said conductor comprises first and second pads on said wiring layer connected by a connection wire.

--14. (new) The semiconductor device according to claim

12, wherein

a first bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said first semiconductor chip;

a second bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said wiring layer; and

a third bonding wire connects another one of said plural bonding pads on said wiring layer to one of said plural bonding pads on said second semiconductor substrate,

said second and third boding wire being electrically connected through said conductor.

--15. (new) The semiconductor device according to claim 12, wherein said wiring layer comprises a lamination of polyimide layer and an aluminum layer.

--16. (new) The semiconductor device according to claim 12, further comprising a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

--17. (new) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first

semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a conductor traversing said wiring layer;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other.

--18. (new) The semiconductor device according to claim 17, further comprising a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

--19. (new) The semiconductor device according to claim 17, wherein said conductor comprises first and second pads on said wiring layer connected by a connection wire.

--20. (new) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a polyimide tape having a copper foil layer therein;